UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,917,662 B2
DATED : July 12, 2005
INVENTOR(S) : Austin et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 2,
Lines 4-6, delete "coupling one the output clock signal of one the frequency divider to a clock output of the programmable divider " and insert -- coupling the output clock signal of one of the frequency dividers to a clock output of the programmable frequency divider --.
Lines 51-52, delete "a schematic a schematic diagram of a frequency a divide by 2" and insert -- a schematic of a frequency divide by 2 --.

Column 4,
Line 10, delete "**115** its output is" and insert -- **115** is --.
Line 56, delete "output (O)" and insert -- output (Q) --.

Column 6,
Line 60, delete "inverting **P12**" and insert -- inverting **P2** --.

Column 9,
Line 58, delete "CLKINMAQXFREQ" and insert -- CLKINMAXFREQ --.

Column 10,
Line 59, delete "FIGS" and insert -- FIG --.
Lines 60 and 64, delete "**166**" and insert -- **I66** --.

Column 11,
Line 22, delete "Buffer **166**" and insert -- Buffer **I66** --.
Line 25, delete "buffer **166**" and insert -- buffer **I66** --.

Column 12,
Line 20, delete "off PFET **T7** off" and insert -- off PFET **T7** --.
Line 37, delete "a schematic a schematic" and insert -- a schematic --.
After line 60, insert the following two paragraphs:
-- In Fig. 9, 2 divider **110** also includes a first inverting multiplexer **345A** and a second inverting multiplexer **345B**. The select input of inverting multiplexer **345A** (**345B**) is coupled to RESET2, a first input of the inverting multiplexer is coupled to ground (VCC) and a second input of the inverting multiplexer is coupled to CLKINB (CLKIN). When RESET2 is high, the output of inverting multiplexer **345A** is high (VCC) and the output of inverting multiplexer **345B** is low (ground). When RESET2 is low, the output of inverting multiplexer **345A** (**345B**) is inverted CLKINB (inverted CLKIN). The output of inverting multiplexer **345A** is coupled to the gate of PFETs **T16** and **T19** and and NFET **T25** (node **P22**). The output of inverting multiplexer **345B** is coupled to the gate of NFETs **T21** and **T18** and PFET **T26** (node **P23**). The drain of PFET **T26** and the source of NFET **T25** are coupled to node **P21**. The source of PFET **T26** and the drain of

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Column 12 (cont'd),
NFET **T25** are coupled together to form a node **P24** hence forming a transmission gate. The gates of PFETs **T15** and **T20** and NFETs **T17** and **T22** are coupled to node **P24**. The 2 divider **110** is completed by a pull down NFET **T25**, the drain of NFET **T27** coupled to node **P21**, the source of NFET **T27** coupled to ground, and the gate of NFET **T27** coupled to RESET2. When RESET2 is high, NFET **T27** is on and node **P21** is pulled low. With node **P21** low, CLKOUT2 is high and no division occurs.
In operation, when RESET2 is high, node **P21** transitions to 0, node **P22** transitions to 1 and node **P23** transitions to 0, PFETs **T16** and **T20** and NFETs **T18** and **T22** are off, nodes **P18** and **P19** hang, NFET **T25** and PFET **T26** are on and **P21=P24=0**. When RESET2 transitions to 0 and if CLKIN=1 and CLKINB=0 then node **P22=1**, node **P23=0**, PFETs **T16** and **T20** and NFETs **T18** and **T22** are off, nodes **P18** and **P19** hang, NFET **T 25** and PFET **T26** are on and **P21=P24=0**. The 2 divider **110** is essentially a divide by 2 state machine for states which transition in the following order. --.

Column 13,
Line 14, delete "*B*24=1" and insert -- **P**24=1 --.

Column 14,
Line 16, delete "a output" and insert -- an output --.
Line 44, delete "geneating" and insert -- generating --.
Lines 65-67, delete "coupling one said output clock signal of one said frequency divider to a clock output of said programmable divider" and insert -- coupling said output clock signal of one of said frequency dividers to a clock output of said programmable frequency dividers --.

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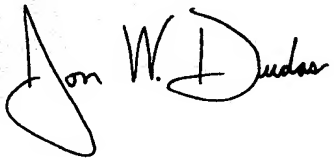
Column 15,
Line 5, delete "output said" and insert -- output of said --.
Line 30, delete "frquency" and insert -- frequency --.

Signed and Sealed this

Twenty-second Day of November, 2005



JON W. DUDAS
Director of the United States Patent and Trademark Office